33.6 A 1.8dB NF 112mW Single-Chip Diversity Tuner for 2.6GHz S-DMB Applications

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"Mobile TV" is recently emerging across the world. In Korean and Japanese markets, a next generation digital broadcasting service, S-DMB system, has been developed for automotive and handheld terminals. Because S-DMB service is mobile and personalized, the market demand is expected to be higher and broader than existing household-based broadcasting services. S-DMB service offers high-quality streaming videos and CD quality music at low cost [1]. S-DMB adopts the code-division multiplexing (CDM) technology and supports the ITU-R BO/1130-4 Digital System E standard. S-DMB service provides extended coverage using a satellite in most areas and gap fillers in shadow areas such as inside buildings and subways. To maximize the coverage with a satellite, a diversity architecture is strongly recommended for the S-DMB tuner by service providers.

Main challenges of an S-DMB tuner are small size, low power consumption, low noise and wide dynamic range. At diversity operating mode, small gain difference and high path isolation between diversity paths are also important constraints over the wide dynamic range. In this paper, a fully monolithic diversity 2.6GHz S-DMB tuner IC is presented. The proposed solution has a die size of 2.3×2.3mm^2, an NF of less than 1.8dB, a path isolation of more than 25dB, and a DR of over 100dB while it has a less than 4dB path-gain mismatch and a power consumption of 112mW.

To reduce size and power consumption for use in battery-operated mobile-TV terminals, two signal path units for diversity architecture are integrated into a single chip with a shared common LO unit, as shown in Fig. 33.6.1. For both signal path units, direct conversion architecture is used to further reduce the size and power consumption. Over 100dB DR, to receive signals from both a satellite and gap fillers, is achieved by the mixed gain-control scheme: wide continuous gain control for the VGA and step gain control for the RF front-end. This step-gain-control scheme is used to achieve lower noise, smaller size, and lower power RF front-end design by eliminating requirements for RF VGA and associated control blocks.

The RF front-end of both signal path units consists of a low-noise step-gain amplifier (LNSGA), a low-noise step-gain down-conversion I/Q mixer (LNSGDCM), and a quadrature LO generator as shown in Fig. 33.6.2. The LNSGA has two gain modes: a high-gain mode and a low-gain mode. For the high-gain mode, an inductively degenerated cascode structure is used to achieve 17dB gain and 1.2dB NF while drawing only 4mA. For the low-gain mode, a digitally adjusted resistor (R1) and a MOS switch (Q3) are used for -13dB loss and over +25dBm IIP3. Coupling between two LNSGA via bonding wires and ground paddle of the package are main causes of degrading path isolation. The path isolation of over 25dB is achieved by reducing the bonding wire coupling factor by careful pin placements, reducing coupling through ground paddle by controlling degeneration amount, and reducing coupling through substrate by careful layout using trench hole. The LNSGDCM has two gain modes: a high-gain mode and a low-gain, which are controlled by resistors array (R2, R7). The high-gain mode has 30dB gain and 5dB NF, and the low-gain mode has 12dB gain and 16dB NF, while consuming 7mA for both modes. The R3 (R4, R8, R9) and C5(C6, C8, C9) simply isolate the transconductance stage (Q4-5, Q10-11) from switching stage (Q6-9, Q12-15) to suppress the harmonics. Even-harmonic reduction loop improves IIP2 immunity performance [2]. The quadrature LO signal is generated using a divide-by-2 circuit from differential signal of the common LO unit to reduce I/Q phase mismatch, dc offset, VCO pushing/pulling, and LO-to-RF radiation.

The baseband part of both signal path units consists of a baseband filter, a VGA, an output buffer, and calibration circuits. The baseband filter is a 5th-order elliptic structure designed for 10MHz bandwidth, 0.5dB ripple, and 40dB attenuation at 15MHz using G_m-C topology. This filter use an on-chip charge-based automatic calibration for filter cutoff frequency over all temperature and process variation [3]. Current steering type VGA is incorporated because of its excellent linear gain in dB characteristic over a wide DR (~60dB), which is critical to achieve simple and accurate RSSI estimation. This is important for the system makers because of the possible cost increase required for extra calibration and complicated look-up table mapping. However, PVT compensation is very critical in dB linearization circuit. In this design, PVT compensation is done through the circuit shown in Fig. 33.6.3, where a PTAT and constant current using a bandgap reference are manipulated to eliminate process and temperature dependencies. Because I/Q and diversity path gain differences must be very small, device sizes are optimized in compensation and linearization circuitry for gain slope matching. A fully monolithic design also improves path matching by better device matching than multi-chip module. Skilled layout technique is also very important to minimize mismatch. Figure 33.6.4(a) shows DR of -100dBm to 0dBm and low path gain difference. Figure 33.6.4(b) shows that the calculated RSSI is well matched over all input range using the mixed gain-control scheme due to the exact dB-linear performance of VGA and step gain performance of LNSGA and LNSGDCM. Figure 33.6.4(c) shows the distribution of path gain difference.

A common LO unit consists of a fractional-N frequency synthesizer and a VCO with AFC. The charge pump (CP) uses a feedback error amplifier to reduce the mismatch between up and down current for lower spurious level and noise. The ΔΣM is designed with a 3rd-order MASH structure having 20b resolution. VCO is based on a standard negative-g_m topology coupled to an LC tank. Cross-coupled NMOS and PMOS core is used for negative g_m to reduce the phase noise. To overcome the temperature and process variation, 4b digital capacitor banks are included, which are calibrated by AFC [4]. As shown in Fig. 33.6.4(d), the in-band phase noise of -75dBc/Hz at 1kHz offset and a noise floor under -127dBc at 1.7MHz offset have been obtained at VCO output while drawing 10mA.

This diversity tuner is implemented in a 0.25μm SiGe BiCMOS technology and the chip micrograph is shown in Fig. 33.6.5. Key parameters are summarized in Fig. 33.6.6. This chip is verified for adoption of S-DMB system using several S-DMB demodulator chips.

References:

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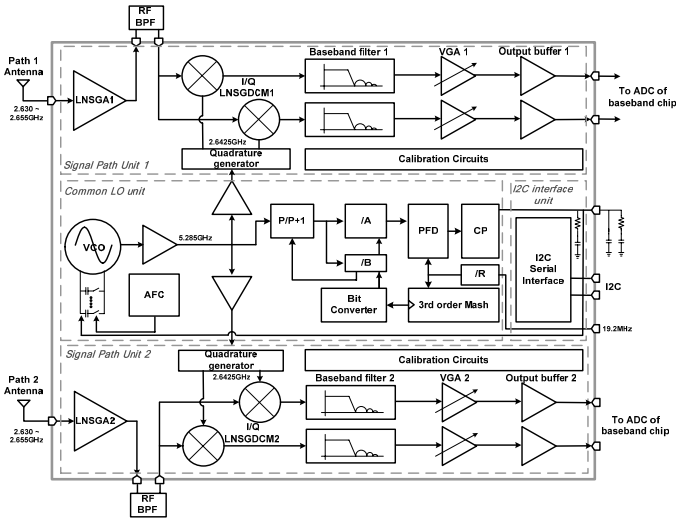

Figure 33.6.1: Block diagram of the proposed diversity tuner for S-DMB.

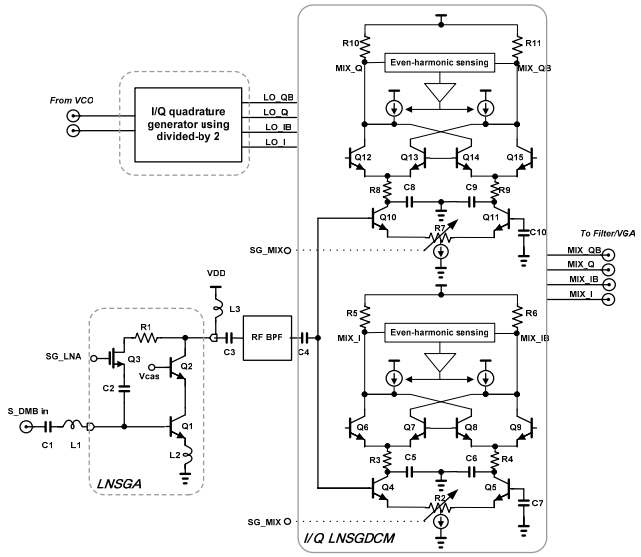

Figure 33.6.2: Simplified RF front-end schematic of thesignal path unit.

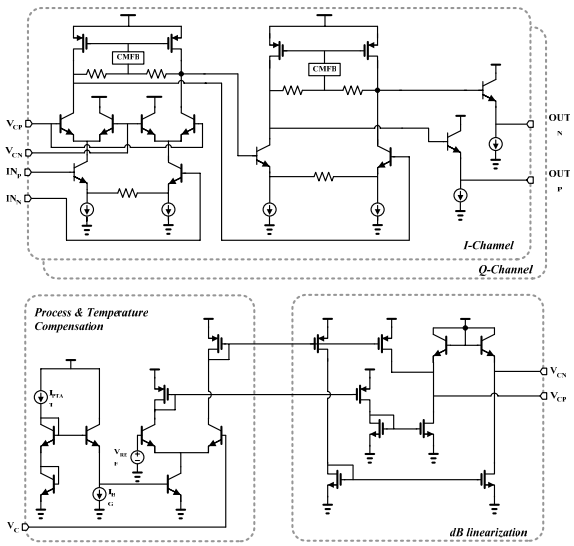

Figure 33.6.3: Simplified VGA schematic of the signal path unit.

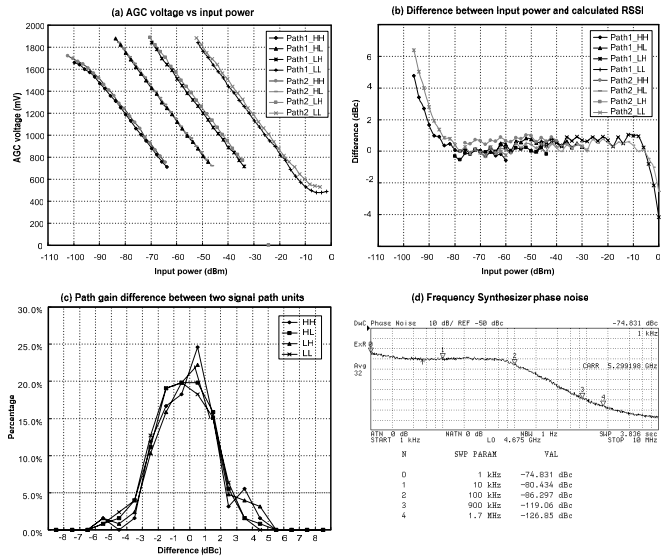

Figure 33.6.4: Measured results.

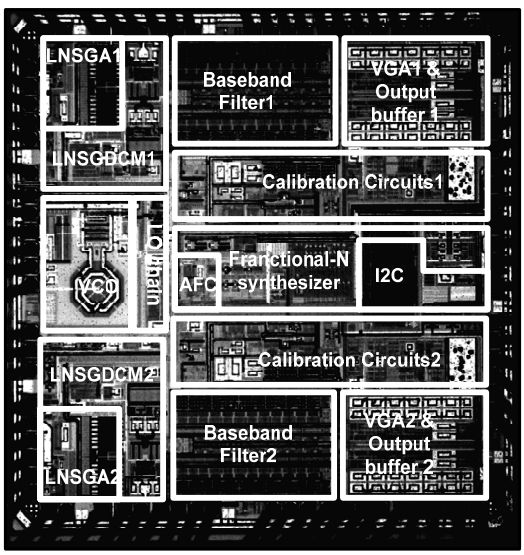

Figure 33.6.5: Die micrograph of the S-DMB chip.

Parameter	Value
Frequnecy	2.630 ~ 2.655GHz
Noise figure @ Max gain	1.8dB
Sensitivity	-100dBm for 2E-4BER
Maximum input level	0dBm
Step gain of LNSGA	30dB
Step gain of LNSGDCM	15dB
VGA control range	> 60dB
BW	10MHz
Attenuation	> 40dBc @ 15MHz
Path isolation	> 25dB
Path gain difference	< 4dB @ 97% yield
Supply voltage	2.5V
Current consumption @ Min gain	44.8mA
Current consumption @ Max gain	55mA

Figure 33.6.6: Performance summary of the tuner.